| | L # | Hits | Search Text | DBs |
|---|---|---|---|---|
| 1 | L2 | 3542 | ((chang$3 alter$3 modif$6 overwrit$3) near10 (instruction code)).ab,ti. | USPAT; US-PGPUB |
| 2 | L4 | 14410 | (chang$3 alter$3 modif$6 overwrit$3) near10 ((instruction code) near20 (memory cache location address)) | USPAT; US-PGPUB |
| 3 | L6 | 2604 | execut$3 near30 4 | USPAT; US-PGPUB |
| 4 | L8 | 522 | (chang$3 alter$3 modif$6 overwrit$3) near10 ((instruction code) near20 (memory cache location address)) near30 execut$3 | EPO; JPO; DERWENT; IBM_TDB |
| 5 | L9 | 22638 | ((chang$3 alter$3 modif$6 overwrit$3) near10 (instruction code)).ab,ti. | EPO; JPO; DERWENT; IBM_TDB |
| 6 | L10 | 458 | 8 and 9 | EPO; JPO; DERWENT; IBM_TDB |
| 7 | L11 | 5 | 8 and patch$3 | EPO; JPO; DERWENT; IBM_TDB |
| 8 | L12 | 2657 | (chang$3 alter$3 modif$6 overwrit$3) near10 ((microinstruction microcode instruction code) near20 (memory cache location address)) near30 execut$3 | USPAT; US-PGPUB |
| 9 | L13 | 3 | 2 and 12 not 7 | USPAT; US-PGPUB |
| 10 | L15 | 423 | (chang$3 alter$3 modif$6 overwrit$3) near10 ((microinstruction microcode instruction code) near10 (memory cache location address)) near10 execut$3 | EPO; JPO; DERWENT; IBM_TDB |
| 11 | L16 | 195 | (chang$3 alter$3 modif$6 overwrit$3) near10 ((microinstruction microcode instruction code) near10 (memory cache location address)) near10 execut$3 | EPO; DERWENT; IBM_TDB |
| 12 | L7 | 385 | 2 and 6 | USPAT; US-PGPUB |
| 13 | L17 | 187 | 7 and @pd<19991006 | USPAT; US-PGPUB |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 1 | US 5963741 A | ☐ | Information processor which rewrites instructions in program to dynamically change program structure and method therefor | 717/111 |
| 2 | US 5963740 A | ☐ | System for monitoring computer system performance | 717/130 |
| 3 | US 5949995 A | ☒ | Programmable branch prediction system and method for inserting prediction operation which is independent of execution of program code | 712/239 |
| 4 | US 5948113 A | ☒ | System and method for centrally handling runtime errors | 714/38 |
| 5 | US 5940859 A | ☒ | Emptying packed data state during execution of packed data instructions | 711/147 |
| 6 | US 5940516 A | ☒ | Data security method and system | 713/159 |
| 7 | US 5938778 A | ☒ | System and method for tracing instructions in an information handling system without changing the system source code | 714/45 |
| 8 | US 5937199 A | ☒ | User programmable interrupt mask with timeout for enhanced resource locking efficiency | 710/262 |
| 9 | US 5933860 A | ☒ | Multiprobe instruction cache with instruction-based probe hint generation and training whereby the cache bank or way to be accessed next is predicted | 711/213 |
| 10 | US 5933626 A | ☒ | Apparatus and method for tracing microprocessor instructions | 712/227 |
| 11 | US 5931957 A | ☒ | Support for out-of-order execution of loads and stores in a processor | 714/48 |
| 12 | US 5930821 A | ☒ | Method and apparatus for shared cache lines in split data/code caches | 711/146 |
| 13 | US 5928358 A | ☒ | Information processing apparatus which accurately predicts whether a branch is taken for a conditional branch instruction, using small-scale hardware | 712/239 |
| 14 | US 5909698 A | ☒ | Cache block store instruction operations where cache coherency is achieved without writing all the way back to main memory | 711/145 |
| 15 | US 5905881 A | ☒ | Delayed state writes for an instruction processor | 712/219 |
| 16 | US 5903760 A | ☒ | Method and apparatus for translating a conditional instruction compatible with a first instruction set architecture (ISA) into a conditional instruction compatible with a second ISA | 717/146 |
| 17 | US 5898864 A | ☒ | Method and system for executing a context-altering instruction without performing a context-synchronization operation within high-performance processors | 712/228 |
| 18 | US 5898850 A | ☒ | Method and system for executing a non-native mode-sensitive instruction within a computer system | 712/229 |
| 19 | US 5895494 A | ☒ | Method of executing perform locked operation instructions for supporting recovery of data consistency if lost due to processor failure, and a method of recovering the data consistency after processor failure | 711/150 |
| 20 | US 5895486 A | ☒ | Method and system for selectively invalidating cache lines during multiple word store operations for memory coherence | 711/121 |
| 21 | US 5893157 A | ☒ | Blocking symbol control in a computer system to serialize accessing a data resource by simultaneous processor requests | 711/150 |
| 22 | US 5889983 A | ☒ | Compare and exchange operation in a processing system | 712/223 |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 23 | US 5875342 A | ☒ | User programmable interrupt mask with timeout | 710/260 |
| 24 | US 5875318 A | ☒ | Apparatus and method of minimizing performance degradation of an instruction set translator due to self-modifying code | 716/3 |
| 25 | US 5862148 A | ☒ | Microcontroller with improved debug capability for internal memory | 714/724 |
| 26 | US 5857096 A | ☒ | Microarchitecture for implementing an instruction to clear the tags of a stack reference register file | 712/229 |
| 27 | US 5845103 A | ☒ | Computer with dynamic instruction reuse | 712/216 |
| 28 | US 5844986 A | ☒ | Secure BIOS | 713/187 |
| 29 | US 5838694 A | ☒ | Dual source data distribution system for integrated circuit tester | 714/738 |
| 30 | US 5835949 A | ☒ | Method of identifying and self-modifying code | 711/135 |
| 31 | US 5835701 A | ☒ | Method and apparatus for modifying relocatable object code files and monitoring programs | 714/35 |
| 32 | US 5829031 A | ☒ | Microprocessor configured to detect a group of instructions and to perform a specific function upon detection | 711/137 |
| 33 | US 5826073 A | ☒ | Self-modifying code handling system | 712/226 |
| 34 | US 5815699 A | ☒ | Configurable branch prediction for a processor performing speculative execution | 712/239 |
| 35 | US 5813039 A | ☒ | Guest execution control system, method and computer process for a virtual machine system | 711/156 |
| 36 | US 5802338 A | ☒ | Method of self-parallelizing and self-parallelizing multiprocessor using the method | 712/217 |
| 37 | US 5796975 A | ☒ | Operand dependency tracking system and method for a processor that executes instructions out of order | 712/218 |
| 38 | US 5790843 A | ☒ | System for modifying microprocessor operations independently of the execution unit upon detection of preselected opcodes | 712/226 |
| 39 | US 5787480 A | ☒ | Lock-up free data sharing | 711/148 |
| 40 | US 5784552 A | ☒ | Debugging a computer program by simulating execution forwards and backwards in a main history log and alternative history logs | 714/38 |
| 41 | US 5781776 A | ☒ | Industrial controller permitting program editing during program execution | 717/130 |
| 42 | US 5765030 A | ☒ | Processor emulator module having a variable pre-fetch queue size for program execution | 714/33 |
| 43 | US 5761490 A | ☒ | Changing the meaning of a pre-decode bit in a cache memory depending on branch prediction mode | 712/239 |
| 44 | US 5761468 A | ☒ | Hardware mechanism for optimizing instruction and data prefetching by forming augmented prefetch instructions | 712/207 |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 45 | US 5758183 A | ☒ | Method of reducing the number of overhead instructions by modifying the program to locate instructions that access shared data stored at target addresses before program execution | 710/5 |
| 46 | US 5758115 A | ☒ | Interoperability with multiple instruction sets | 712/209 |
| 47 | US 5742791 A | ☒ | Apparatus for detecting updates to instructions which are within an instruction processing pipeline of a microprocessor | 711/146 |
| 48 | US 5740442 A | ☒ | Method and apparatus for identifying and correcting date calculation errors caused by truncated year values | 717/124 |
| 49 | US 5737636 A | ☒ | Method and system for detecting bypass errors in a load/store unit of a superscalar processor | 710/54 |
| 50 | US 5732273 A | ☒ | System for monitoring compute system performance | 717/128 |
| 51 | US 5732268 A | ☒ | Extended BIOS adapted to establish remote communication for diagnostics and repair | 713/2 |
| 52 | US 5732254 A | ☒ | Pipeline system branch history table storing branch instruction addresses and target addresses with inhibit bits | 712/240 |
| 53 | US 5729757 A | ☒ | Super-computer system architectures using status memory to alter program | 712/1 |
| 54 | US 5724563 A | ☒ | Pipeline processsor | 712/233 |
| 55 | US 5717587 A | ☒ | Method and system for recording noneffective instructions within a data processing system | 700/2 |
| 56 | US 5715454 A | ☒ | Version control of documents by independent line change packaging | 707/203 |
| 57 | US 5701506 A | ☒ | Microcomputer having ROM program which can be altered | 712/37 |
| 58 | US 5692168 A | ☒ | Prefetch buffer using flow control bit to identify changes of flow within the code stream | 712/237 |
| 59 | US 5692167 A | ☒ | Method for verifying the correct processing of pipelined instructions including branch instructions and self-modifying code in a microprocessor | 712/226 |
| 60 | US 5682528 A | ☒ | Spoon-feed initialization in a multiprocessor system | 713/1 |
| 61 | US 5680597 A | ☒ | System with flexible local control for modifying same instruction partially in different processor of a SIMD computer system to execute dissimilar sequences of instructions | 712/226 |
| 62 | US 5671231 A | ☒ | Method and apparatus for performing cache snoop testing on a cache system | 714/724 |
| 63 | US 5668947 A | ☒ | Microprocessor self-test apparatus and method | 714/30 |
| 64 | US 5666507 A | ☒ | Pipelined microinstruction apparatus and methods with branch prediction and speculative state changing | 712/218 |
| 65 | US 5655132 A | ☒ | Register file with multi-tasking support | 718/104 |
| 66 | US 5655096 A | ☒ | Method and apparatus for dynamic scheduling of instructions to ensure sequentially coherent data in a processor employing out-of-order execution | 712/200 |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 67 | US 5652852 A | ☒ | Processor for discriminating between compressed and non-compressed program code, with prefetching, decoding and execution of compressed code in parallel with the decoding, with modified target branch addresses accommodated at run time | 712/208 |
| 68 | US 5649137 A | ☒ | Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency | 712/207 |
| 69 | US 5644769 A | ☒ | System for optimizing program by virtually executing the instruction prior to actual execution of the program to invalidate unnecessary instructions | 717/154 |
| 70 | US 5644744 A | ☒ | Superscaler instruction pipeline having boundary identification logic for variable length instructions | 712/207 |
| 71 | US 5640526 A | ☒ | Superscaler instruction pipeline having boundary indentification logic for variable length instructions | 712/207 |
| 72 | US 5636366 A | ☒ | System and method for preserving instruction state-atomicity for translated program | 711/163 |
| 73 | US 5625787 A | ☒ | Superscalar instruction pipeline using alignment logic responsive to boundary identification logic for aligning and appending variable length instructions to instructions stored in cache | 712/204 |
| 74 | US 5619680 A | ☒ | Methods and apparatus for concurrent execution of serial computing instructions using combinatorial architecture for program partitioning | 711/173 |
| 75 | US 5619408 A | ☒ | Method and system for recoding noneffective instructions within a data processing system | 712/226 |
| 76 | US 5613078 A | ☒ | Microprocessor and microprocessor system with changeable effective bus width | 710/307 |
| 77 | US 5602536 A | ☒ | Data synchronization method for use with portable, microprocessor-based device | 340/5.23 |
| 78 | US 5596738 A | ☒ | Peripheral device control system using changeable firmware in a single flash memory | 711/103 |
| 79 | US 5594880 A | ☒ | System for executing a plurality of tasks within an instruction in different orders depending upon a conditional value | 712/245 |
| 80 | US 5586278 A | ☒ | Method and apparatus for state recovery following branch misprediction in an out-of-order microprocessor | 712/235 |
| 81 | US 5584027 A | ☒ | Method and apparatus for finding induction variables for use in compiling computer instructions | 717/160 |
| 82 | US 5581720 A | ☒ | Apparatus and method for updating information in a microcode instruction | 712/226 |
| 83 | US 5546554 A | ☒ | Apparatus for dynamic register management in a floating point unit | 711/203 |
| 84 | US 5542084 A | ☒ | Method and apparatus for executing an atomic read-modify-write instruction | 345/501 |
| 85 | US 5539907 A | ☒ | System for monitoring computer system performance | 717/130 |
| 86 | US 5535329 A | ☒ | Method and apparatus for modifying relocatable object code files and monitoring programs | 714/35 |
| 87 | US 5522084 A | ☒ | Method and system for invalidating instructions utilizing validity and write delay flags in parallel processing apparatus | 712/23 |
| 88 | US 5511207 A | ☒ | Program control circuit determining the designated number of times a sequence of instructions is repetitively executed to prevent further execution of a jump instruction | 712/241 |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 89 | US 5511175 A | ☒ | Method an apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency | 712/216 |
| 90 | US 5504901 A | ☒ | Position independent code location system | 717/144 |
| 91 | US 5504859 A | ☒ | Data processor with enhanced error recovery | 714/11 |
| 92 | US 5479620 A | ☒ | Control unit modifying micro instructions for one cycle execution | 712/226 |
| 93 | US 5465361 A | ☒ | Microcode linker/loader that generates microcode sequences for MRI sequencer by modifying previously generated microcode sequences | 717/168 |
| 94 | US 5463743 A | ☒ | Method of improving SCSI operations by actively patching SCSI processor instructions | 710/105 |
| 95 | US 5454117 A | ☒ | Configurable branch prediction for a processor performing speculative execution | 712/23 |
| 96 | US 5454075 A | ☒ | Device and method for multiple display system having storage means for enlarged images | 345/536 |
| 97 | US 5446876 A | ☒ | Hardware mechanism for instruction/data address tracing | 714/47 |
| 98 | US 5440704 A | ☒ | Data processor having branch predicting function | 712/239 |
| 99 | US 5440703 A | ☒ | System and method for saving state information in a multi-execution unit processor when interruptable instructions are identified | 712/228 |
| 100 | US 5428786 A | ☒ | Branch resolution via backward symbolic execution | 717/151 |
| 101 | US 5418916 A | ☒ | Central processing unit checkpoint retry for store-in and store-through cache systems | 712/228 |
| 102 | US 5408672 A | ☒ | Microcomputer having ROM to store a program and RAM to store changes to the program | 712/37 |
| 103 | US 5392207 A | ☒ | Programmable motion controller with graphical programming aid | 700/64 |
| 104 | US 5359730 A | ☒ | Method of operating a data processing system having a dynamic software update facility | 717/169 |
| 105 | US 5345567 A | ☒ | System and method for modifying program status word system mask, system access key, and address space code with overlap enabled | 712/228 |
| 106 | US 5335344 A | ☒ | Method for inserting new machine instructions into preexisting machine code to monitor preexisting machine access to memory | 714/35 |
| 107 | US 5317743 A | ☒ | System for compiling iterated loops based on the possibility of parallel execution | 717/160 |
| 108 | US 5317740 A | ☒ | Alternate and iterative analysis of computer programs for locating translatable code by resolving callbacks and other conflicting mutual dependencies | 717/129 |
| 109 | US 5303358 A | ☒ | Prefix instruction for modification of a subsequent instruction | 712/226 |
| 110 | US 5301302 A | ☒ | Memory mapping and special write detection in a system and method for simulating a CPU processor | 703/20 |
| 111 | US 5301295 A | ☒ | Data processor apparatus and method with selective caching of instructions | 711/125 |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 112 | US 5274815 A | ☒ | Dynamic instruction modifying controller and operation method | 712/226 |
| 113 | US 5269017 A | ☒ | Type 1, 2 and 3 retry and checkpointing | 714/15 |
| 114 | US 5226132 A | ☒ | Multiple virtual addressing using/comparing translation pairs of addresses comprising a space address and an origin address (STO) while using space registers as storage devices for a data processing system | 711/209 |
| 115 | US 5226130 A | ☒ | Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency | 712/238 |
| 116 | US 5214770 A | ☒ | System for flushing instruction-cache only when instruction-cache address and data-cache address are matched and the execution of a return-from-exception-or-interrupt command | 711/123 |
| 117 | US 5197135 A | ☒ | Memory management for scalable compound instruction set machines with in-memory compounding | 712/217 |
| 118 | US 5193180 A | ☒ | System for modifying relocatable object code files to monitor accesses to dynamically allocated memory | 717/163 |
| 119 | US 5185880 A | ☒ | Stored instructions executing type timing signal generating system | 713/500 |
| 120 | US 5168560 A | ☒ | Microprocessor system private split cache tag stores with the system tag store having a different validity bit for the same data line | 711/123 |
| 121 | US 5167026 A | ☒ | Simultaneously or sequentially decoding multiple specifiers of a variable length pipeline instruction based on detection of modified value of specifier registers | 712/210 |
| 122 | US 5163146 A | ☒ | System responsive to interrupt levels for changing and restoring clock speed by changing and restoring a register value | 713/501 |
| 123 | US 5148530 A | ☒ | Method for reexecuting instruction by altering high bits of instruction address based upon result of a subtraction operation with stored low bits | 711/220 |
| 124 | US 5142631 A | ☒ | System for queuing individual read or write mask and generating respective composite mask for controlling access to general purpose register | 712/217 |
| 125 | US 5142630 A | ☒ | System for calculating branch destination address based upon address mode bit in operand before executing an instruction which changes the address mode and branching | 712/234 |
| 126 | US 5136714 A | ☒ | Method and apparatus for implementing inter-processor interrupts using shared memory storage in a multi-processor computer system | 710/260 |
| 127 | US 5093783 A | ☒ | Microcomputer register bank accessing | 711/220 |
| 128 | US 5081462 A | ☒ | Method of deriving phase of pseudo-random code signal in global positioning system receiver | 342/352 |
| 129 | US 5038280 A | ☒ | Information processing apparatus having address expansion function | 712/237 |
| 130 | US 4992977 A | ☒ | Cache memory device constituting a memory device used in a computer | 711/143 |
| 131 | US 4982358 A | ☒ | High speed programmable controller for executing an instruction formed by a ladder | 345/467 |
| 132 | US 4970679 A | ☒ | Pulse input apparatus | 341/122 |
| 133 | US 4962463 A | ☒ | Video imaging device with image altering controls and related method | 715/500.1 |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 134 | US 4958632 A | ☒ | Adaptable, digital computer controlled cardiac pacemaker | 607/11 |
| 135 | US 4914584 A | ☒ | Rules and apparatus for an intermediate code memory that buffers code segments | 712/237 |
| 136 | US 4879646 A | ☒ | Data processing system with a pipelined structure for editing trace memory contents and tracing operations during system debugging | 712/227 |
| 137 | US 4835679 A | ☒ | Microprogram control system | 712/212 |
| 138 | US 4825360 A | ☒ | System and method for parallel processing with mostly functional languages | 718/106 |
| 139 | US 4825355 A | ☒ | Instruction format for program control type data processing systems | 712/224 |
| 140 | US 4794522 A | ☒ | Method for detecting modified object code in an emulator | 703/26 |
| 141 | US 4792996 A | ☒ | Information medium for communicating data and/or a selectable control transfer program between the medium end and external device | 398/140 |
| 142 | US 4766538 A | ☒ | Microprocessor having variable data width | 710/307 |
| 143 | US 4760519 A | ☒ | Data processing apparatus and method employing collision detection and prediction | 712/217 |
| 144 | US 4742466 A | ☒ | System for measuring path coverage represented by the degree of passage of execution paths in a program | 714/45 |
| 145 | US 4731742 A | ☒ | Video display control system | 345/572 |
| 146 | US 4675810 A | ☒ | Digital data processing system having a uniquely organized memory system using object-based addressing and in which operand data is identified by names accessed by name tables | 711/202 |
| 147 | US 4638452 A | ☒ | Programmable controller with dynamically altered programmable real time interrupt interval | 710/266 |
| 148 | US 4636941 A | ☒ | Method and apparatus for analysis of microprocessor operation | 714/25 |
| 149 | US 4625294 A | ☒ | Table-driven apparatus for data display and modification | 715/530 |
| 150 | US 4611281 A | ☒ | Apparatus for analyzing microprocessor operation | 714/39 |
| 151 | US 4602347 A | ☒ | Microcomputer addressing system and electronic timepiece utilizing the same | 702/178 |
| 152 | US 4584640 A | ☒ | Method and apparatus for a compare and swap instruction | 707/200 |
| 153 | US 4558411 A | ☒ | Polymorphic programmable units employing plural levels of sub-instruction sets | 712/37 |
| 154 | US 4538225 A | ☒ | Table-driven apparatus for data display and modification | 715/530 |
| 155 | US 4516203 A | ☒ | Improved apparatus for encaching data whose value does not change during execution of an instruction sequence | 711/3 |
| 156 | US 4500959 A | ☒ | Apparatus for invalidating the content of an instruction buffer by program store compare check | 712/207 |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 157 | US 4494114 A | ☒ | Security arrangement for and method of rendering microprocessor-controlled electronic equipment inoperative after occurrence of disabling event | 340/5.31 |
| 158 | US 4466057 A | ☒ | Digital data processing system respoonsive to instructions containing operation code modifiers | 712/210 |
| 159 | US 4459664 A | ☒ | Multiprocessor computer system with dynamic allocation of multiprocessing tasks and processor for use in such multiprocessor computer system | 718/105 |
| 160 | US 4454579 A | ☒ | System for performing call and return operations | 712/242 |
| 161 | US 4449185 A | ☒ | Implementation of instruction for a branch which can cross one page boundary | 712/234 |
| 162 | US 4439830 A | ☒ | Computer system key and lock protection mechanism | 711/164 |
| 163 | US 4434464 A | ☒ | Memory protection system for effecting alteration of protection information without intervention of control program | 711/164 |
| 164 | US 4410959 A | ☒ | Computer control system for selecting a desired control program from a plurality of control programs | 187/247 |
| 165 | US 4409654 A | ☒ | Data processor adapted for interruption to an instruction stream | 711/213 |
| 166 | US 4354231 A | ☒ | Apparatus for reducing the instruction execution time in a computer employing indirect addressing of a data memory | 711/220 |
| 167 | US 4316245 A | ☒ | Apparatus and method for semaphore initialization in a multiprocessing computer system for process synchronization | 718/106 |
| 168 | US 4315314 A | ☒ | Priority vectored interrupt having means to supply branch address directly | 712/244 |
| 169 | US 4306285 A | ☒ | Data processing apparatus | 712/226 |
| 170 | US 4287561 A | ☒ | Address formulation interlock mechanism | 712/217 |
| 171 | US 4250545 A | ☒ | Data processing apparatus providing autoloading of memory pointer registers | 712/208 |
| 172 | US 4240142 A | ☒ | Data processing apparatus providing autoincrementing of memory pointer registers | 712/42 |
| 173 | US 4195339 A | ☒ | Sequential control system | 712/234 |
| 174 | US 4184201 A | ☒ | Integrating processor element | 710/36 |
| 175 | US 4103326 A | ☒ | Time-slicing method and apparatus for disk drive | 718/107 |
| 176 | US 4095278 A | ☒ | Instruction altering system | 712/226 |
| 177 | US 3984813 A | ☒ | Microprocessor system | 712/40 |
| 178 | US 3983541 A | ☒ | Polymorphic programmable units employing plural levels of phased sub-instruction sets | 712/247 |
| 179 | US 3983539 A | ☒ | Polymorphic programmable units employing plural levels of sub-instruction sets | 712/247 |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 180 | US 3959777 A | ☒ | Data processor for pattern recognition and the like | 712/234 |
| 181 | US 3827029 A | ☒ | MEMORY AND PROGRAM PROTECTION SYSTEM FOR A DIGITAL COMPUTER SYSTEM | 711/163 |
| 182 | US 3781823 A | ☒ | COMPUTER CONTROL UNIT CAPABLE OF DYNAMICALLY REINTERPRETING INSTRUCTIONS | 712/209 |
| 183 | US 3778775 A | ☒ | MICROPROGRAMMED TERMINAL | 712/245 |
| 184 | US 3764988 A | ☒ | INSTRUCTION PROCESSING DEVICE USING ADVANCED CONTROL SYSTEM | 712/234 |
| 185 | US 3737867 A | ☒ | DIGITAL COMPUTER WITH ACCUMULATOR SIGN BIT INDEXING | 712/226 |
| 186 | US 3718912 A | ☒ | INSTRUCTION EXECUTION UNIT | 712/217 |
| 187 | US 3597739 A | ☒ | METHOD FOR OPERATING A DATA PROCESSOR | 711/200 |

| | L # | Hits | Search Text | DBs |
|---|---|---|---|---|
| 1 | L2 | 3542 | ((chang$3 alter$3 modif$6 overwrit$3) near10 (instruction code)).ab,ti. | USPAT; US-PGPUB |
| 2 | L4 | 14410 | (chang$3 alter$3 modif$6 overwrit$3) near10 ((instruction code) near20 (memory cache location address)) | USPAT; US-PGPUB |
| 3 | L6 | 2604 | execut$3 near30 4 | USPAT; US-PGPUB |
| 4 | L8 | 522 | (chang$3 alter$3 modif$6 overwrit$3) near10 ((instruction code) near20 (memory cache location address)) near30 execut$3 | EPO; JPO; DERWENT; IBM_TDB |
| 5 | L9 | 22638 | ((chang$3 alter$3 modif$6 overwrit$3) near10 (instruction code)).ab,ti. | EPO; JPO; DERWENT; IBM_TDB |
| 6 | L10 | 458 | 8 and 9 | EPO; JPO; DERWENT; IBM_TDB |
| 7 | L11 | 5 | 8 and patch$3 | EPO; JPO; DERWENT; IBM_TDB |
| 8 | L12 | 2657 | (chang$3 alter$3 modif$6 overwrit$3) near10 ((microinstruction microcode instruction code) near20 (memory cache location address)) near30 execut$3 | USPAT; US-PGPUB |
| 9 | L13 | 3 | 2 and 12 not 7 | USPAT; US-PGPUB |
| 10 | L15 | 423 | (chang$3 alter$3 modif$6 overwrit$3) near10 ((microinstruction microcode instruction code) near10 (memory cache location address)) near10 execut$3 | EPO; JPO; DERWENT; IBM_TDB |
| 11 | L16 | 195 | (chang$3 alter$3 modif$6 overwrit$3) near10 ((microinstruction microcode instruction code) near10 (memory cache location address)) near10 execut$3 | EPO; DERWENT; IBM_TDB |
| 12 | L7 | 385 | 2 and 6 | USPAT; US-PGPUB |
| 13 | L17 | 187 | 7 and @pd<19991006 | USPAT; US-PGPUB |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 1 | WO 9854639 A1 | ☐ | PATCHING APPARATUS AND METHOD FOR UPGRADING MODEM SOFTWARE CODE | |
| 2 | US 6691308 B | ☐ | Hot patch circuit for changing micro code to be executed in processor, has cache system that selectively compares, for each address generated by program counter, generated address to addresses stored in cache system | |
| 3 | US 20030028757 A | ☐ | Instructions modifying method for uniprocessor system, involves overwriting memory location with value representing patch class instruction concurrent with execution of another value representing patch class instruction | |
| 4 | EP 1280056 A | ☐ | Linking object code modules to form executable program by deriving call frame information instructions from call frame information macros | |
| 5 | US 6317870 B | ☐ | Inter-module procedure call optimization for computer program, involves modifying call instruction to directly call unresolved module at determined location, once unresolved module is called during program execution | |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 1 | US 20040 06471 5 A1 | ☐ | Method and device for accessing a memory to prevent tampering of a program in the memory | 713/193 |
| 2 | US 20040 06468 5 A1 | ☒ | System and method for real-time tracing and profiling of a superscalar processor implementing conditional execution | 712/227 |
| 3 | US 20040 05970 6 A1 | ☒ | System and method for providing concurrent usage and replacement of non-native language codes | 707/1 |
| 4 | US 20040 04977 0 A1 | ☒ | Infrastructure for generating a downloadable, secure runtime binary image for a secondary processor | 717/162 |
| 5 | US 20040 04966 3 A1 | ☒ | System with wide operand architecture and method | 712/222 |
| 6 | US 20040 04965 4 A1 | ☒ | Secondary processor execution kernel framework | 712/35 |
| 7 | US 20040 04501 8 A1 | ☒ | Using address space bridge in postoptimizer to route indirect calls at runtime | 719/331 |
| 8 | US 20040 03484 5 A1 | ☒ | Code conversion method and apparatus | 717/100 |
| 9 | US 20040 03095 3 A1 | ☒ | Fault-tolerant architecture for in-circuit programming | 714/10 |
| 10 | US 20040 01988 6 A1 | ☒ | Compilation of application code in a data processing apparatus | 717/158 |
| 11 | US 20040 01977 0 A1 | ☒ | Optimization apparatus, compiler program, optimization method and recording medium | 712/227 |
| 12 | US 20040 01592 2 A1 | ☒ | Program preparation apparatus | 717/154 |
| 13 | US 20040 01567 5 A1 | ☒ | SMC detection and reverse translation in a translation lookaside buffer | 711/207 |
| 14 | US 20030 23338 6 A1 | ☒ | High speed virtual machine and compiler | 718/100 |
| 15 | US 20030 22977 7 A1 | ☒ | Use of hashing in a secure boot loader | 713/2 |
| 16 | US 20030 22599 3 A1 | ☒ | Computer system | 711/202 |
| 17 | US 20030 21298 3 A1 | ☒ | Method and system for modifying executable code to add additional functionality | 717/110 |

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|---|---|---|---|---|
| 18 | US 20030 20470 5 A1 | ☒ | Prediction of branch instructions in a data processing apparatus | 712/207 |
| 19 | US 20030 20467 3 A1 | ☒ | Data prefetching apparatus in a data processing system and method therefor | 711/137 |
| 20 | US 20030 19179 2 A1 | ☒ | High speed virtual machine and compiler | 718/100 |
| 21 | US 20030 15901 9 A1 | ☒ | Prediction of instructions in a data processing apparatus | 712/207 |
| 22 | US 20030 14033 8 A1 | ☒ | Method, apparatus and article for generation of debugging information | 717/162 |
| 23 | US 20030 14022 2 A1 | ☒ | System for managing circuitry of variable function information processing circuit and method for managing circuitry of variable function information processing circuit | 713/1 |
| 24 | US 20030 10129 2 A1 | ☒ | System and method for isolating applications from each other | 719/328 |
| 25 | US 20030 09755 1 A1 | ☒ | System and method for a deploying a hardware configuration with a computer program | 713/1 |
| 26 | US 20030 09738 2 A1 | ☒ | Identifying changed records in a file stored on an electronic token | 707/204 |
| 27 | US 20030 08443 3 A1 | ☒ | Profile-guided stride prefetching | 717/158 |
| 28 | US 20030 08422 9 A1 | ☒ | Methods and apparatus for modifying programs stored in read only memory | 711/102 |
| 29 | US 20030 08408 9 A1 | ☒ | Data transfer apparatus | 709/200 |
| 30 | US 20030 04666 2 A1 | ☒ | Data reproduction apparatus | 717/115 |
| 31 | US 20030 04649 4 A1 | ☒ | Program control flow conditioned on presence of requested data in cache memory | 711/138 |
| 32 | US 20030 04122 5 A1 | ☒ | Mechanism for handling load lock/store conditional primitives in directory-based distributed shared memory multiprocessors | 712/30 |
| 33 | US 20030 03722 3 A1 | ☒ | Apparatus and method for ownership load locked misses for atomic lock acquisition in a multiprocessor computer system | 712/28 |
| 34 | US 20030 03359 2 A1 | ☒ | Software debugger and software development support system | 717/128 |

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|---|---|---|---|---|
| 35 | US 20030028757 A1 | ☒ | Concurrent modification and execution of instructions | 712/226 |
| 36 | US 20030023964 A1 | ☒ | System and method for compacting field upgradeable wireless communication device software code sections | 717/172 |
| 37 | US 20030018906 A1 | ☒ | Method and system for protecting software applications against static and dynamic software piracy techniques | 713/189 |
| 38 | US 20020199067 A1 | ☒ | System and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model | 711/145 |
| 39 | US 20020194545 A1 | ☒ | Method of testing embedded memory array and embedded memory controller for use therewith | 714/42 |
| 40 | US 20020194454 A1 | ☒ | Method and arrangement for instruction word generation in the driving of functional units in a processor | 712/24 |
| 41 | US 20020184399 A1 | ☒ | Interpreting functions utilizing a hybrid of virtual and native machine instructions | 719/310 |
| 42 | US 20020184179 A1 | ☒ | Method and system for distributing product information | 707/1 |
| 43 | US 20020172082 A1 | ☒ | Method and apparatus for changing region code of digital versatile disc drive | 365/200 |
| 44 | US 20020163935 A1 | ☒ | System and method for providing transformation of multi-protocol packets in a data stream | 370/466 |
| 45 | US 20020157042 A1 | ☒ | Algorithmically programmable memory tester with breakpoint trigger, error jamming and 'scope mode that memorizes target sequences | 714/45 |
| 46 | US 20020147901 A1 | ☒ | Method of handling instructions within a processor with decoupled architecture, in particular a processor for digital signal processing, and corresponding processor | 712/225 |
| 47 | US 20020144245 A1 | ☒ | Static compilation of instrumentation code for debugging support | 717/140 |
| 48 | US 20020144241 A1 | ☒ | Debugging support using dynamic re-compilation | 717/136 |
| 49 | US 20020124158 A1 | ☒ | Virtual r0 register | 712/226 |
| 50 | US 20020120923 A1 | ☒ | Method for software pipelining of irregular conditional control loops | 717/160 |
| 51 | US 20020116663 A1 | ☒ | Data processing system with on-chip FIFO for storing debug information and method therefor | 714/30 |

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|---|---|---|---|---|
| 52 | US 20020116597 A1 | ☒ | Memory accelerator for ARM processors | 712/207 |
| 53 | US 20020112149 A1 | ☒ | Data processor and method of operation | 712/236 |
| 54 | US 20020104077 A1 | ☒ | Multi-threaded fragment patching | 717/162 |
| 55 | US 20020100028 A1 | ☒ | System for modifying the functionality of compiled computer code at run-time | 717/139 |
| 56 | US 20020093574 A1 | ☒ | Digital camera | 348/231.6 |
| 57 | US 20020091963 A1 | ☒ | Fault-tolerant architecture for in-circuit programming | 714/2 |
| 58 | US 20020087925 A1 | ☒ | Computer processor read/alter/rewrite optimization cache invalidate signals | 714/718 |
| 59 | US 20020087846 A1 | ☒ | Reconfigurable processing system and method | 712/229 |
| 60 | US 20020087810 A1 | ☒ | System and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model | 711/145 |
| 61 | US 20020073398 A1 | ☒ | METHOD AND SYSTEM FOR MODIFYING EXECUTABLE CODE TO ADD ADDITIONAL FUNCTIONALITY | 717/110 |
| 62 | US 20020066910 A1 | ☒ | Semiconductor integrated circuit | 257/200 |
| 63 | US 20020062479 A1 | ☒ | Microcontroller with modifiable program | 717/168 |
| 64 | US 20020049865 A1 | ☒ | Direct invocation of methods using class loader | 719/315 |
| 65 | US 20020046298 A1 | ☒ | INTERPRETING FUNCTIONS UTILIZING A HYBRID OF VIRTUAL AND NATIVE MACHINE INSTRUCTIONS | 719/310 |
| 66 | US 20020032879 A1 | ☒ | Fault-tolerant architecture for in-circuit programming | 714/2 |
| 67 | US 20020029357 A1 | ☒ | Method and system of memory management using stack walking | 714/9 |
| 68 | US 20020004897 A1 | ☒ | Data processing apparatus for executing multiple instruction sets | 712/227 |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 69 | US 20020 00257 3 A1 | ☒ | Processor with reconfigurable arithmetic data path | 708/501 |
| 70 | US 20010 04746 9 A1 | ☒ | Emptying packed data state during execution of packed data instructions | 712/229 |
| 71 | US 20010 03749 7 A1 | ☒ | Apparatus and method for generating optimization objects | 717/160 |
| 72 | US 20010 02753 8 A1 | ☒ | Computer register watch | 714/28 |
| 73 | US 20010 02533 8 A1 | ☒ | Systems and methods for transient error recovery in reduced instruction set computer processors via instruction retry | 712/228 |
| 74 | US 20010 02097 8 A1 | ☒ | Electronic camera | 348/222 .1 |
| 75 | US 20010 00712 4 A1 | ☒ | Program modification device | 711/165 |
| 76 | US 20010 00475 7 A1 | ☒ | Processor and method of controlling the same | 712/218 |
| 77 | US 67185 45 B1 | ☒ | Apparatus for managing resources of a signal processor, a resource managing program transferring method and recording medium | 717/168 |
| 78 | US 67150 51 B2 | ☒ | Program modification device | 711/165 |
| 79 | US 67049 25 B1 | ☒ | Dynamic binary translator with a system and method for updating and maintaining coherency of a translation cache | 717/138 |
| 80 | US 66912 46 B1 | ☒ | System and method of processing partially defective memories | 714/8 |
| 81 | US 66869 04 B1 | ☒ | Wheel reporting method for a personal computer keyboard interface | 345/168 |
| 82 | US 66788 86 B2 | ☒ | Apparatus and method for generating optimization objects | 717/151 |
| 83 | US 66752 98 B1 | ☒ | Execution of instructions using op code lengths longer than standard op code lengths to encode data | 713/190 |
| 84 | US 66717 98 B1 | ☒ | Configurable branch prediction for a processor performing speculative execution | 712/234 |
| 85 | US 66683 72 B1 | ☒ | Software profiling method and apparatus | 717/130 |
| 86 | US 66614 18 B1 | ☒ | Character animation system | 345/473 |
| 87 | US 66473 01 B1 | ☒ | Process control system with integrated safety control system | 700/79 |
| 88 | US 66369 50 B1 | ☒ | Computer architecture for shared memory access | 711/147 |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 89 | US 6629241 B1 | ☒ | Data processing apparatus with non-volatile memory for both program and data | 713/100 |
| 90 | US 6629209 B1 | ☒ | Cache coherency protocol permitting sharing of a locked data granule | 711/141 |
| 91 | US 6625701 B1 | ☒ | Extended cache coherency protocol with a modified store instruction lock release indicator | 711/152 |
| 92 | US 6618824 B1 | ☒ | Method and apparatus for modifying relocatable object code files and monitoring programs | 714/35 |
| 93 | US 6616358 B1 | ☒ | Keyboard structure alteration method | 400/472 |
| 94 | US 6615333 B1 | ☒ | Data processing device, method of executing a program and method of compiling | 711/169 |
| 95 | US 6615304 B1 | ☒ | Processing unit in which access to system memory is controlled | 710/260 |
| 96 | US 6611900 B2 | ☒ | System and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model | 711/145 |
| 97 | US 6598166 B1 | ☒ | Microprocessor in which logic changes during execution | 713/190 |
| 98 | US 6594821 B1 | ☒ | Translation consistency checking for modified target instructions by comparing to original copy | 717/136 |
| 99 | US 6594734 B1 | ☒ | Method and apparatus for self modifying code detection using a translation lookaside buffer | 711/146 |
| 100 | US 6571329 B1 | ☒ | Detection of overwrite modification by preceding instruction possibility of fetched instruction code using fetched instructions counter and store target address | 712/205 |
| 101 | US 6560641 B1 | ☒ | System, method, and adapter card for remote console emulation including remote control of a peripheral device | 709/219 |
| 102 | US 6539500 B1 | ☒ | System and method for tracing | 714/45 |
| 103 | US 6536034 B1 | ☒ | Method for modifying code sequences and related device | 717/110 |
| 104 | US 6523095 B1 | ☒ | Method and data processing system for using quick decode instructions | 711/144 |
| 105 | US 6513156 B2 | ☒ | Interpreting functions utilizing a hybrid of virtual and native machine instructions | 717/151 |
| 106 | US 6510351 B1 | ☒ | Modifier function blocks in a process control system | 700/18 |
| 107 | US 6505295 B1 | ☒ | Data processor | 712/241 |
| 108 | US 6502176 B1 | ☒ | Computer system and methods for loading and modifying a control program without stopping the computer system using reserve areas | 711/170 |
| 109 | US 6467084 B1 | ☒ | Systems and methods for reprogramming an embedded device with program code using relocatable program code | 717/136 |
| 110 | US 6463511 B2 | ☒ | System and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model | 711/145 |
| 111 | US 6425074 B1 | ☒ | Method and apparatus for rapid execution of FCOM and FSTSW | 712/222 |

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|---|---|---|---|---|
| 112 | US 6418514 B1 | ☒ | Removal of posted operations from cache operations queue | 711/133 |
| 113 | US 6415360 B1 | ☒ | Minimizing self-modifying code checks for uncacheable memory types | 711/139 |
| 114 | US 6405316 B1 | ☒ | Method and system for injecting new code into existing application code | 713/190 |
| 115 | US 6405307 B1 | ☒ | Apparatus and method for detecting and handling self-modifying code conflicts in an instruction fetch pipeline | 712/239 |
| 116 | US 6401221 B1 | ☒ | Fault-tolerant architecture for in-circuit programming | 714/36 |
| 117 | US 6401196 B1 | ☒ | Data processor system having branch control and method thereof | 712/241 |
| 118 | US 6393556 B1 | ☒ | Apparatus and method to change processor privilege without pipeline flush | 712/229 |
| 119 | US 6389512 B1 | ☒ | Microprocessor configured to detect updates to instructions outstanding within an instruction processing pipeline and computer system including same | 711/125 |
| 120 | US 6382846 B1 | ☒ | Intermediate instruction execution processor which resolves symbolic references without modifying intermediate instruction code | 712/209 |
| 121 | US 6381679 B1 | ☒ | Information processing system with prefetch instructions having indicator bits specifying cache levels for prefetching | 711/137 |
| 122 | US 6374333 B1 | ☒ | Cache coherency protocol in which a load instruction hint bit is employed to indicate deallocation of a modified cache line supplied by intervention | 711/145 |
| 123 | US 6360318 B1 | ☒ | Configurable branch prediction for a processor performing speculative execution | 712/240 |
| 124 | US 6360194 B1 | ☒ | Different word size multiprocessor emulation | 703/26 |
| 125 | US 6356918 B1 | ☒ | Method and system for managing registers in a data processing system supports out-of-order and speculative instruction execution | 707/203 |
| 126 | US 6347361 B1 | ☒ | Cache coherency protocols with posted operations | 711/141 |
| 127 | US 6345340 B1 | ☒ | Cache coherency protocol with ambiguous state for posted operations | 711/141 |
| 128 | US 6343280 B1 | ☒ | Distributed execution software license server | 705/55 |
| 129 | US 6339560 B1 | ☒ | Semiconductor memory based on address transitions | 365/233.5 |
| 130 | US 6336212 B1 | ☒ | Self modifying code to test all possible addressing modes | 717/124 |
| 131 | US 6330643 B1 | ☒ | Cache coherency protocols with global and local posted operations | 711/141 |
| 132 | US 6317870 B1 | ☒ | System and method for optimization of inter-module procedure calls | 717/151 |
| 133 | US 6317868 B1 | ☒ | Process for transparently enforcing protection domains and access control as well as auditing operations in software components | 717/127 |
| 134 | US 6308261 B1 | ☒ | Computer system having an instruction for probing memory latency | 712/219 |

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|---|---|---|---|---|
| 135 | US 6298481 B1 | ☒ | System for modifying the functionality of compiled computer code at run-time | 717/110 |
| 136 | US 6285974 B1 | ☒ | Hardware verification tool for multiprocessors | 703/13 |
| 137 | US 6282675 B1 | ☒ | Fault-tolerant architecture for in-circuit programming | 714/36 |
| 138 | US 6282639 B1 | ☒ | Configurable branch prediction for a processor performing speculative execution | 712/240 |
| 139 | US 6266486 B1 | ☒ | Emptying packed data state during execution of packed data instructions | 708/204 |
| 140 | US 6256777 B1 | ☒ | Method and apparatus for debugging of optimized machine code, using hidden breakpoints | 717/129 |
| 141 | US 6249906 B1 | ☒ | Adaptive method and system to minimize the effect of long table walks | 717/153 |
| 142 | US 6247118 B1 | ☒ | Systems and methods for transient error recovery in reduced instruction set computer processors via instruction retry | 712/228 |
| 143 | US 6247036 B1 | ☒ | Processor with reconfigurable arithmetic data path | 708/603 |
| 144 | US 6240546 B1 | ☒ | Identifying date fields for runtime year 2000 system solution process, method and article of manufacture | 717/131 |
| 145 | US 6240506 B1 | ☒ | Expanding instructions with variable-length operands to a fixed length | 712/213 |
| 146 | US 6237088 B1 | ☒ | System and method for tracking in-flight instructions in a pipeline | 712/239 |
| 147 | US 6237076 B1 | ☒ | Method for register renaming by copying a 32 bits instruction directly or indirectly to a 64 bits instruction | 712/23 |
| 148 | US 6206484 B1 | ☒ | Method and apparatus for modifying relocatable object code files and monitoring programs | 714/35 |
| 149 | US 6199139 B1 | ☒ | Refresh period control apparatus and method, and computer | 711/106 |
| 150 | US 6195756 B1 | ☒ | Power reduction for multiple-instruction-word processors by modification of instruction words | 713/340 |
| 151 | US 6192517 B1 | ☒ | Method, apparatus, and product for improved garbage collection in a memory system through the removal of reference conflicts | 717/154 |
| 152 | US 6185674 B1 | ☒ | Method and apparatus for reconstructing the address of the next instruction to be completed in a pipelined processor | 712/230 |
| 153 | US 6178549 B1 | ☒ | Memory writer with deflective memory-cell handling capability | 717/124 |
| 154 | US 6178484 B1 | ☒ | DCBST with ICBI mechanism to maintain coherency of bifurcated data and instruction caches | 711/145 |
| 155 | US 6173421 B1 | ☒ | Centrally handling runtime errors | 714/38 |
| 156 | US 6170082 B1 | ☒ | Taking corrective action in computer programs during instruction processing | 717/127 |
| 157 | US 6145059 A | ☒ | Cache coherency protocols with posted operations and tagged coherency states | 711/143 |

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| 158 | US 61417 68 A | ☒ | Self-corrective memory system and method | 714/8 |
| 159 | US 61416 98 A | ☒ | Method and system for injecting new code into existing application code | 719/331 |
| 160 | US 61380 59 A | ☒ | Vehicle control system and unit for preventing power supply cutoff during re-programming mode | 701/1 |
| 161 | US 61356 51 A | ☒ | Patching apparatus and method for upgrading modem software code | 717/168 |
| 162 | US 61311 45 A | ☒ | Information processing unit and method for controlling a hierarchical cache utilizing indicator bits to control content of prefetching operations | 711/137 |
| 163 | US 61287 71 A | ☒ | System and method for automatically modifying database access methods to insert database object handling instructions | 717/111 |
| 164 | US 61287 27 A | ☒ | Self modifying code to test all possible addressing modes | 712/227 |
| 165 | US 61287 10 A | ☒ | Method utilizing a set of blocking-symbol resource-manipulation instructions for protecting the integrity of data in noncontiguous data objects of resources in a shared memory of a multiple processor computer system | 711/152 |
| 166 | US 61184 49 A | ☒ | Server system and method for modifying a cursor image | 345/861 |
| 167 | US 61122 80 A | ☒ | Method and apparatus for distinct instruction pointer storage in a partitioned cache memory | 711/129 |
| 168 | US 61087 97 A | ☒ | Method and system for loading microprograms in partially defective memory | 714/8 |
| 169 | US 61087 77 A | ☒ | Configurable branch prediction for a processor performing speculative execution | 712/240 |
| 170 | US 61065 73 A | ☒ | Apparatus and method for tracing microprocessor instructions | 717/128 |
| 171 | US 61015 82 A | ☒ | Dcbst with icbi mechanism | 711/141 |
| 172 | US 60918 96 A | ☒ | Debugging optimized code using data change points | 717/125 |
| 173 | US 60885 25 A | ☒ | Loop profiling by instrumentation | 717/150 |
| 174 | US 60853 33 A | ☒ | Method and apparatus for synchronization of code in redundant controllers in a swappable environment | 714/7 |
| 175 | US 60818 86 A | ☒ | Holding mechanism for changing operation modes in a pipelined computer | 712/229 |
| 176 | US 60759 37 A | ☒ | Preprocessing of stored target routines for controlling emulation of incompatible instructions on a target processor and utilizing target processor feedback for controlling non-sequential incompatible instruction emulation | 703/23 |
| 177 | US 60732 17 A | ☒ | Method for detecting updates to instructions which are within an instruction processing pipeline of a microprocessor | 711/146 |
| 178 | US 60552 11 A | ☒ | Force page zero paging scheme for microcontrollers using data random access memory | 365/238 .5 |
| 179 | US 60527 71 A | ☒ | Microprocessor with pipeline synchronization | 712/34 |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 180 | US 6047367 A | ☒ | Microprocessor with improved out of order support | 712/23 |
| 181 | US 6047125 A | ☒ | Garbage collection system for improved use of memory by removal of reference conflicts | 717/148 |
| 182 | US 6044453 A | ☒ | User programmable circuit and method for data processing apparatus using a self-timed asynchronous control structure | 712/201 |
| 183 | US 6026237 A | ☒ | System and method for dynamic modification of class files | 717/130 |
| 184 | US 6023758 A | ☒ | Method and processor for changing program by replacing instruction stored in ROM with predetermined value to be interpreted as an instruction | 712/220 |
| 185 | US 6021481 A | ☒ | Effective-to-real address cache managing apparatus and method | 711/207 |
| 186 | US 6021265 A | ☒ | Interoperability with multiple instruction sets | 712/209 |
| 187 | US 6009516 A | ☒ | Pipelined microprocessor with efficient self-modifying code detection and handling | 712/244 |
| 188 | US 6002881 A | ☒ | Coprocessor data access control | 712/34 |
| 189 | US 6000014 A | ☒ | Software-managed programmable congruence class caching mechanism | 711/128 |
| 190 | US 5999732 A | ☒ | Techniques for reducing the cost of dynamic class initialization checks in compiled code | 717/148 |
| 191 | US 5996071 A | ☒ | Detecting self-modifying code in a pipelined processor with branch processing by comparing latched store address to subsequent target address | 712/238 |
| 192 | US 5995102 A | ☒ | Server system and method for modifying a cursor image | 345/856 |
| 193 | US 5974538 A | ☒ | Method and apparatus for annotating operands in a computer system with source instruction identifiers | 712/218 |
| 194 | US 5974240 A | ☒ | Method and system for buffering condition code data in a data processing system having out-of-order and speculative instruction execution | 712/218 |
| 195 | US 5968174 A | ☒ | Method and apparatus for implementing a 32-bit operating system which supports 16-bit code | 713/2 |
| 196 | US 5968135 A | ☒ | Processing instructions up to load instruction after executing sync flag monitor instruction during plural processor shared memory store/load access synchronization | 709/400 |
| 197 | US 5965730 A | ☒ | Structure and method for instruction boundary machine state restoration | 712/244 |
| 198 | US 5964893 A | ☒ | Data processing system for performing a trace function and method therefor | 714/39 |
| 199 | US 5963741 A | ☒ | Information processor which rewrites instructions in program to dynamically change program structure and method therefor | 717/111 |
| 200 | US 5963740 A | ☐ | System for monitoring computer system performance | 717/130 |

| | L # | Hits | Search Text | DBs |
|---|---|---|---|---|
| 1 | L2 | 3542 | ((chang$3 alter$3 modif$6 overwrit$3) near10 (instruction code)).ab,ti. | USPAT; US-PGPUB |
| 2 | L4 | 14410 | (chang$3 alter$3 modif$6 overwrit$3) near10 ((instruction code) near20 (memory cache location address)) | USPAT; US-PGPUB |
| 3 | L6 | 2604 | execut$3 near30 4 | USPAT; US-PGPUB |
| 4 | L8 | 522 | (chang$3 alter$3 modif$6 overwrit$3) near10 ((instruction code) near20 (memory cache location address)) near30 execut$3 | EPO; JPO; DERWENT; IBM_TDB |
| 5 | L9 | 22638 | ((chang$3 alter$3 modif$6 overwrit$3) near10 (instruction code)).ab,ti. | EPO; JPO; DERWENT; IBM_TDB |
| 6 | L10 | 458 | 8 and 9 | EPO; JPO; DERWENT; IBM_TDB |
| 7 | L11 | 5 | 8 and patch$3 | EPO; JPO; DERWENT; IBM_TDB |
| 8 | L12 | 2657 | (chang$3 alter$3 modif$6 overwrit$3) near10 ((microinstruction microcode instruction code) near20 (memory cache location address)) near30 execut$3 | USPAT; US-PGPUB |
| 9 | L13 | 3 | 2 and 12 not 7 | USPAT; US-PGPUB |
| 10 | L15 | 423 | (chang$3 alter$3 modif$6 overwrit$3) near10 ((microinstruction microcode instruction code) near10 (memory cache location address)) near10 execut$3 | EPO; JPO; DERWENT; IBM_TDB |
| 11 | L16 | 195 | (chang$3 alter$3 modif$6 overwrit$3) near10 ((microinstruction microcode instruction code) near10 (memory cache location address)) near10 execut$3 | EPO; DERWENT; IBM_TDB |
| 12 | L7 | 385 | 2 and 6 | USPAT; US-PGPUB |
| 13 | L17 | 187 | 7 and @pd<19991006 | USPAT; US-PGPUB |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 1 | US 5475852 A | ☐ | Microprocessor implementing single-step or sequential microcode execution while in test mode | 714/34 |
| 2 | US 5345570 A | ☐ | Microprogram control circuit | 712/248 |
| 3 | US 4707661 A | ☐ | Machine generation of machine-executable state-change instructions for magnetic resonance imaging | 324/309 |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 1 | EP 1365308 A2 | ☐ | Method and apparatus for minimizing differential power attacks on processors | |
| 2 | WO 2086652 A1 | ☒ | PROCESSOR | |
| 3 | EP 1109096 A2 | ☒ | Processor and method of controlling the same | |
| 4 | FR 2789193 A1 | ☒ | Method for modifying behavior of computer under execution of functions in binary code by replacing first branching instruction by second branching instruction at first determined address | |
| 5 | EP 997787 A2 | ☒ | Image forming apparatus for managing copy sheets individually | |
| 6 | EP 889393 A2 | ☒ | Force page zero paging scheme for microcontrollers | |
| 7 | WO 9854639 A1 | ☒ | PATCHING APPARATUS AND METHOD FOR UPGRADING MODEM SOFTWARE CODE | |
| 8 | WO 9837467 A1 | ☒ | PERSONAL COMPUTER-INCORPORATED NUMERICAL CONTROL APPARATUS, AND IMAGE TRANSFER METHOD FOR PERSONAL COMPUTER-INCORPORATED NUMERICAL CONTROL APPARATUSES | |
| 9 | EP 785504 A2 | ☒ | Out of order execution of load instructions in a superscalar processor | |
| 10 | EP 736830 A1 | ☒ | Method and apparatus for reconstructing the address of the next instruction to be completed in a pipelined processor | |
| 11 | EP 696772 A2 | ☒ | Register file with multi-tasking support | |
| 12 | EP 597441 A1 | ☒ | Microprocessor having a bus-width change function. | |
| 13 | EP 431326 A2 | ☒ | Inter-processor interrupts in an n-element multi-processor. | |
| 14 | EP 327195 A2 | ☒ | Processor simulation. | |
| 15 | FR 2582421 A1 | ☒ | Identity authentication apparatus | |
| 16 | EP 202628 A2 | ☒ | Instruction monitor used for a stored-program data processor. | |
| 17 | WO 8605015 A1 | ☒ | MICROPROGRAM CONTROLLER | |
| 18 | GB 2040519 A | ☒ | Improvements in or Relating to Data Processing Systems | |
| 19 | GB 2016753 A | ☒ | Data Processing System | |
| 20 | NN82014018 | ☒ | Instruction Execution Conditioned on Operand Addresses. January 1982. | |
| 21 | NN71022505 | ☒ | Re Enterable Programming. February 1971. | |
| 22 | US 20040025165 A | ☒ | Operating system functionality extending method for supporting new protocol, involves determining if functionality is to be modified to execute code stored by dynamic execution layer interface, to implement modified functionality | |

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| 23 | US 6691308 B | ☒ | Hot patch circuit for changing micro code to be executed in processor, has cache system that selectively compares, for each address generated by program counter, generated address to addresses stored in cache system | |
| 24 | JP 2004049433 A | ☒ | Game machine e.g. pachinko machine controls display of special specific presentation display in scrolling game from series of continuous presentation display, based on determination result | |
| 25 | US 20040019770 A | ☒ | Optimization apparatus for computer, has generation unit which generates dummy instruction and controller that performs optimization by changing execution instruction order over dummy instruction | |
| 26 | CN 1447244 A | ☒ | Method designed in CPU for detecting buffer area overflow | |
| 27 | US 20030208696 A | ☒ | Computer system stores encoded password and configuration data in read only memory, which are modified by system management interrupt-based code executed by central processing unit | |
| 28 | US 6631520 B | ☒ | Execution code changing method of microcontroller, involves loading overlay code in second page of memory, asserting overlay flags for selected portions of default code and substituting overlay code in those portions | |
| 29 | US 6625701 B | ☒ | Data processing method in multiprocessor data processing system, involves modifying contents of memory corresponding to selected address, by executing stored conditional instruction | |
| 30 | US 20030167423 A | ☒ | Program product for testing consistency of machine code and source files, has instructions executed to produce source file attribute record including file location information, file modified date, during compilation of file source code | |
| 31 | US 20030145314 A | ☒ | Program optimizing method in network computer, involves modifying program to be executed to include optimized sequence of instructions comprising prefetch instructions, when cache misses occurs | |
| 32 | JP 2003198362 A | ☒ | Processing system for general-purpose computer, has shift register with field programmable gate array data memories storing respective modules of large scale program, of which appropriate one is selected and executed | |
| 33 | US 20030084229 A | ☒ | Read only memory program modification method for embedded systems, involves modifying code segments of read only memory by executing replacement code segment of random access memory | |
| 34 | US 6549989 B | ☒ | Cache coherency management method in multiprocessor data processing system, involves indicating reservation continuing and releasing states of selected address, during modification of contents of associated cache | |
| 35 | US 20030069016 A | ☒ | Recorded medium stores instruction for executing return of acknowledgement, on reception of address change machine of mobile host over secured control channel | |
| 36 | US 20030067473 A | ☒ | Predefined code set execution method for programmable vertex shader, involves executing specified substitute instructions using intermediate result obtained by executing another instruction using not more than n input operands | |
| 37 | US 6550058 B | ☒ | Computer executable code generation method for multitask program stack management, involves inserting stack clearing code in return operations for clearing stack memory to prevent usage of residual data in stack | |
| 38 | JP 2003068019 A | ☒ | Optical disk apparatus includes comparator which compares key code for overwriting stored in buffer memory and key code stored in non-volatile memory | |
| 39 | US 20030046622 A | ☒ | Data reproduction apparatus used in e.g. electronic publishing, has script analysis and execution unit that controls data reproduction according to specified reproduction instruction | |

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| 40 | US 20030 02875 7 A | ☒ | Instructions modifying method for uniprocessor system, involves overwriting memory location with value representing patch class instruction concurrent with execution of another value representing patch class instruction | |
| 41 | US 20030 00521 2 A | ☒ | Stored program modification method for use in PC, involves invoking address match routine to execute portion of correction code during program execution | |
| 42 | JP 20030 67152 A | ☒ | Image processor e.g. printer, facsimile, scanner, copier, has rewriting instruction unit that provides instructions to firmware rewriting unit to overwrite firmware stored in memory | |
| 43 | FR 28283 05 A | ☒ | Protection of software against unauthorized use, reproduction or alteration, e.g. for protection of chip card software or software protected by a material key associated with a USB port using a principle of a verification variable | |
| 44 | GB 23790 57 A | ☒ | Memory operations testing method for computer program development detects accesses to unmapped region of two-region virtual memory associated with physical memory | |
| 45 | EP 12800 56 A | ☒ | Linking object code modules to form executable program by deriving call frame information instructions from call frame information macros | |
| 46 | US 20020 19906 7 A | ☒ | Locked-memory instruction execution method in multi-threaded processor system, involves merging modified version of load data value and stored load data value, when un-snooped condition of cacheline is determined | |
| 47 | US 20020 17413 6 A | ☒ | Database management system optimization method involves updating summary table in solid state disk, corresponding to manipulations of data in reconstructed tables | |
| 48 | WO 20028 9146 A | ☒ | Testing an embedded memory array, an instruction or a series of consecutively executed instructions are repeated with modifications to the instruction fields of each command, specific instructions have an active repeat control field | |
| 49 | WO 20028 6652 A | ☒ | Processor has instruction decoder that issues an instruction to a data path block | |
| 50 | US 20020 15698 1 A | ☒ | System management RAM implementation method in computer systems, involves caching extended memory by changing cache settings using write-back and uncaching SMRAM upon execution of resume instruction | |
| 51 | WO 20027 7822 A | ☒ | Monitoring run time execution of software code by inserting routine into buffer with data or cache disabling instruction | |
| 52 | US 20020 12082 9 A | ☒ | Data processor for cellular phone, has buffer controller circuit that validates flag of buffer, when instruction is prefetched into that buffer | |
| 53 | US 20020 11214 9 A | ☒ | Program execution method in data processing system, involves selecting jump address by comparing output of program counter with preset value | |
| 54 | US 20020 09193 4 A | ☒ | Encrypted viral code decryption detection method for computer virus detection, involves detecting modification to flagged memory area during emulation of specific instruction in completely executable code | |
| 55 | US 20020 08781 0 A | ☒ | Locked-memory instruction execution method in microprocessor, involves merging modified load data value with stored load data value after determination of unsnooped condition of cacheline | |
| 56 | US 20020 07332 3 A | ☒ | Virus detection method in computer system involves monitoring emulation of computer executable code and modification of memory state to detect attempt by emulated code to access restricted computer system resources | |
| 57 | US 20020 04630 5 A | ☒ | Foreign binary code translating system for computer, stores page tables representing memory allocation in response to changes generated by executing binary translated codes | |

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| 58 | TW 480396 A | ☒ | Method capable of simultaneously storing program code and data in flash memory - capable of greatly improving data modification efficiency of flash memory | |
| 59 | US 6356918 B | ☒ | Register array management method in data processing system, involves storing instruction execution result in address acquired from rename table, and moving next address from completion table to rename table | |
| 60 | US 6349366 B | ☒ | Memory management system for multiprocessor shared memory system, outputs probe command through system port to target processor, so that state of data block of processor is changed in accordance with probe command | |
| 61 | US 6336212 B | ☒ | Software application for testing addressing modes in microprocessor, modifies test code which executes several instructions, to test incremented addressing mode and initializes data used by addressing modes | |
| 62 | US 6317870 B | ☒ | Inter-module procedure call optimization for computer program, involves modifying call instruction to directly call unresolved module at determined location, once unresolved module is called during program execution | |
| 63 | US 2001003232 7 A | ☒ | Memory processing method for microcontroller, involves selecting object code having matching skipped-code-address range based on detection result of defective addresses in memory and loading into memory for execution | |
| 64 | WO 2001756 05 A | ☒ | Debugging an executing service on pipelined CPU architecture, involves setting break point including altering instruction within execution service and invalidating page cache of the execution service | |
| 65 | CN 1308337 A | ☒ | Simultaneous program code and data storing method in flash memory | |
| 66 | US 2001001007 2 A | ☒ | Instruction translator for non-native instructions for processor, has selector for selectively outputting instruction output by translator and corresponding instruction held in instruction cache | |
| 67 | CN 1303043 A | ☒ | Basic cache block microprocessor changes execution of instructions, based on instruction history information showing exception event relating to instruction group | |
| 68 | EP 1111510 A | ☒ | Program modification device for computer system, has instruction switch which replaces program data and addresses, in order to make execution unit read modification target program data instead of source address data | |
| 69 | JP 2001166935 A | ☒ | Branch instruction address estimation procedure for processor, involves executing branch instructions sequentially, by judging validity of the assigned addresses | |
| 70 | US 2001004757 A | ☒ | Processor that performs a load operation prior to a store operation while avoiding ambiguous memory reference, and achieves high-speed operations using history control unit for controlling out-of-order processes | |
| 71 | US 6243807 B | ☒ | Computer architecture performance optimization method involves retrieving function information as single block from external memory into cache memory when executing loop routine | |
| 72 | US 6243789 B | ☒ | Program code execution in dynamic random access memory, involves resuming program execution, after copying and remapping page of flash EEPROM, attempted to be modified by program, to RAM | |
| 73 | US 6237088 B | ☒ | In-flight instruction tracking apparatus in pipeline of microprocessor, compares line address associated with fetched instruction in pipeline, with address of stored instruction, to detect SMC conflict | |
| 74 | JP 2001092663 A | ☒ | Data processor of sto add program type digital computer, processes memory access instruction by dynamically changing the execution time and calculation instruction according to execution time determined statically | |
| 75 | SE 0000447 A | ☒ | Encryption device, used to encrypt information packets comprising non encrypted text data block and block header | |

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| 76 | WO 20011 4965 A | ☒ | Data processor transfers control from subprogram stored in auxiliary memory to various instructions in memory temporarily after suspending data change and before change is completed | |
| 77 | KR 20010 03246 A | ☒ | Method for managing feature codes using shared memory in home location register | |
| 78 | WO 20006 8784 A | ☒ | Data processing device for executing load instructions, modifies data handling, and primary and secondary memory access instruction programs command to compensate out of order execution of memory access instruction | |
| 79 | US 61287 27 A | ☒ | Addressing mode testing of microprocessor, involves using self modifying code so that test instruction executed to test one addressing mode is modified to use for next testing | |
| 80 | JP 20002 42484 A | ☒ | Control program modification method for computer system, involves dividing execution code and data code during first stage loading on main memory unit | |
| 81 | US 61087 97 A | ☒ | Automatic program code modification method for memory chips, involves bypassing dummy codes by inserting jump instruction to obtain modified program code | |
| 82 | JP 20002 22242 A | ☒ | Compilation of Java program in network computing, involves storing address of execution code which changes stack pointer and information about size of stack frame after change, in memory | |
| 83 | FR 27891 93 A | ☒ | Method for modifying behavior of computer under execution of functions in binary code by replacing first branching instruction by second branching instruction at first determined address | |
| 84 | US 20020 02934 6 A | ☒ | Conditional jump operation masking in cryptographic processor, involves executing different number of instructions for each conditional jump, for each evaluation of distinguishing value against reference value | |
| 85 | US 60732 17 A | ☒ | Instruction update snooping method for superscalar microprocessors, involves deleting address from buffer for updating instructions, if inequality occurs in address stored in buffer and update address | |
| 86 | US 60556 31 A | ☒ | Booting method for personal digital assistant | |
| 87 | US 60498 66 A | ☒ | User mode cache synchronization for MIPS architecture computer system, involves changing certain entries of instruction cache in specific address range as invalid during cache synchronization instruction execution | |
| 88 | JP 20000 47863 A | ☒ | Information processor for video game apparatus, generates jump instruction to the address where the modified part of program is stored in external memory | |
| 89 | US 59912 00 A | ☒ | Erasing control circuit for batch erasable type EEPROM, flash EPROM in microcomputer system | |
| 90 | US 59499 73 A | ☒ | Stack override prevention method of computer operating system | |
| 91 | US 59408 59 A | ☒ | Floating point and packed data instructions execution method for multimedia applications | |
| 92 | JP 11143 597 A | ☒ | Microprocessor - has low power consumption decision circuit that outputs low power consumption mode signal which changes microprocessor or power save mode circuit into low power consumption condition | |
| 93 | US 59058 81 A | ☒ | Delayed state write apparatus for memory in pipelined instruction processor of data processing system | |
| 94 | US 58976 65 A | ☒ | Register addressing for register architecture used for microprocessor, microcontroller | |

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| 95 | RD 419119 A | ☒ | Suspending threads at safe points - involves suspending thread until handler is called for thread execution | |
| 96 | JP 11065843 A | ☒ | Microprocessor for pipeline processing - changes order of execution according to dependence of prefetched instruction with instruction stored in memory | |
| 97 | US 5881276 A | ☒ | Manipulation of protected pages to reduce conditional statements usage in coded program | |
| 98 | US 5881272 A | ☒ | Parallel processors synchronization system for image and graphics processing system | |
| 99 | JP 11039150 A | ☒ | Micro controller - has CPU which executes control program stored in flash memory during change of mode based on input specific instruction code which does not change program counter value | |
| 100 | US 6044435 A | ☒ | Machine readable storage device embodying instructions executable by memory controller of memory management subsystem - tests if modifications made to lists of tape drives available to serve requests in modified request queue allow n different drives to be assigned to n requests | |
| 101 | JP 11015793 A | ☒ | Simultaneous instruction execution method in computer system - involves setting resources order wise so as to prevent its modification during instruction execution by adjacent processors, based on usability or non-usability of resources lock status | |
| 102 | US 5862385 A | ☒ | Compiling method for program execution in computer - involves compiling reordered intermediate code into object code and is ultimately executed which generates less cache conflicts than that of when initial intermediate code is compiled and executed | |
| 103 | JP 10340210 A | ☒ | Task debug apparatus for operating system - interrupts process of T system for corresponding task and address when output signals of address event detector output controller and instruction execution event detector are in active condition | |
| 104 | WO 9857255 A | ☒ | Modification of code sequences. - using active orientation instructions to obtain time delay after which rerouting to new address takes place. | |
| 105 | US 5838694 A | ☒ | Dual source data distribution system for integrated circuit tester - has distributed memories to store test vectors and central control to instruct execution or altering of test vectors | |
| 106 | US 5835949 A | ☒ | Pipelined microprocessor for computer system - flushes execution pipeline in response to instruction written to address within primary instruction cache | |
| 107 | EP 871125 A | ☒ | Logic module e.g. for implementing system changes on PC architecture computers - has transceiver module and memory module containing storage elements and executable code stored as pages with logic card having page register module in communication with transceiver and memory | |
| 108 | US 5812133 A | ☒ | Industrial controller for mixing tank - has address monitor that alters display of graphical element when electronic memory is accessed by address corresponding to identified graphic element | |
| 109 | US 5802573 A | ☒ | Data processing system execution simulation method - involves initializing target locations and storing them in queues corresponding to store instruction and load instruction | |
| 110 | JP 10105537 A | ☒ | Simulation system with facility for modifying setting parameters during simulation program execution - includes shared memory in which instructions input by input-output interface unit are stored and later read out to execute simulation program corresponding to changed parameter | |
| 111 | RD 408092 A | ☒ | Propagating memory cache hits and misses to software - using control bit in processor to modify manner in which memory load instructions are executed | |

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| 112 | US 5729757 A | ☒ | Super computer system architecture using status memory to alter program - has instruction sequencing under program control computer, with individual instructions assigned for execution to individual instruction computer, and modifiable micro-tasks to execute instruction between successive or during single cycle | |
| 113 | US 5717587 A | ☒ | Method of recording non-effective instruction in data processing system - involves re-coding selected instruction into specified instruction format prior to further processing of selected instruction | |
| 114 | JP 10020907 A | ☒ | Sequence control method for designing and modification of sequence circuit - involves executing instruction of lower order module using input-output address of control object obtained by converting command from higher order module with reference to address parameter table | |
| 115 | EP 810517 A | ☒ | Hardware mechanism for avoiding thrashing caused by data or instruction prefetched to cache memory - has prefetch instruction buffer which is communication with prefetch execution unit for storing augmented prefetch instructions for retrieval at execution of prefetch instruction | |
| 116 | JP 09311786 A | ☒ | Data processor e.g. microprocessor, microcomputer - executes instruction of second instruction format which is altered from instruction of first instruction format stored in instruction memory | |
| 117 | US 5655096 A | ☒ | Pipelined program execution method with exception handling - involves dynamically determining instruction execution point when instructions are executed in non-sequential program order knowing when previous source location writes and reads and writes of destination locations will be completed | |
| 118 | US 5640560 A | ☒ | Method of modifying multimedia recorded on non-volatile medium e.g CD-ROM - involves transferring machine instructions that implement filter to memory of computer that is to execute multimedia work for execution by computer | |
| 119 | TW 302445 A | ☒ | Load queue for bypassing in a load/store unit of a superscalar processor - includes real page number buffer for storing real page numbers for instruction entries in queue nad real page number comparator for comparing executing load instructions with queued load instruction entries | |
| 120 | EP 749063 A | ☒ | Code execution control method for suspend/resume operation in computer - using multiple suspend files to save multiple system states, and multiple operating systems requiring multiple swap files | |
| 121 | EP 740248 A | ☒ | Responding to trapping conditions in pipelined computer - involves distinguishing between hardware traps and software traps, forwarding software trapping instruction to execute stage and changing fetch address | |
| 122 | JP 08106383 A | ☒ | Operation processor e.g. microprocessor, digital signal processor - provided with control signal output by first and second decoder for RISC and CISC after scanning command setting from memory based on execution of clock and performs operation processing after receiving data directly from memory | |
| 123 | JP 08030307 A | ☒ | Controlled system processes order controller for vegetable growing hot house temp. - has value replaced by back-and-front process and starting order and changed automatically with changed setting time displayed on operation display | |
| 124 | GB 2290395 A | ☒ | Data processing appts with multiple program instruction function - has controller that controls processor core to execute program instruction word in response to predetermine indicator bit of program counter register | |
| 125 | US 5475852 A | ☒ | Pipeline microprocessor - includes test mode for executing whole microprogram routine and one microinstruction of arbitrary address in micro ROM to diagnose internal functions and unit for changing sequence field and executes between two continuous instruction | |
| 126 | US 5469550 A | ☒ | Reversible computer instruction execution unit - has CPU with microinstruction memory programmed to support forward and reverse execution instructions with restoration of data values overwritten by forward instruction if needed | |

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| 127 | US 5581720 A | ☒ | Information updating circuit for microcode instruction without interrupting program execution - periodically accesses instruction for execution from memory and selectively alters program information within microcode instruction stored in memory | |
| 128 | JP 07264471 A | ☒ | Special effect device with switch maintaining execution speed of key frame - has rotary control changing execution speed of key frame stored in memory controlled by entered instructions NoAbstract | |
| 129 | GB 2287334 A | ☒ | Maintaining memory consistency in pipeline, non-blocking caching bus request queue - includes external bus request queue for ensuring that request to same address are issued and serviced on bus according to set memory ordering scheme | |
| 130 | EP 737334 B | ☒ | Pipelined micro-instruction system with branch prediction and speculative changing - uses multi-stage pipelining and branch prediction to enable speculative changes of state during execution of predicted instruction before determining prediction accuracy | |
| 131 | US 5410685 A | ☒ | Non-intrusive method for recovering state of computer system - using memory having two matched levels, with checkpoint instructions causing target processor to cue checkpoint processor to initiate checkpoint process | |
| 132 | EP 640916 A | ☒ | Microcomputer with instruction executing unit and program memory - has executing unit and program memory with counter successively indicating addresses to output contents through interface with comparator giving selection signal if true | |
| 133 | US 5392207 A | ☒ | Method of programming motion controller for control of industrial servo-motors - requires initially selecting graphical icons, each icon representing sequential step in control of motor, and displaying on electronic display | |
| 134 | US 5377336 A | ☒ | Pre-fetching data for load instruction before transfer to execution unit - processing data fetch in load instructions in load unit which predicts address for data fetch such that fetch can occur earlier than in typical load processing | |
| 135 | US 5345567 A | ☒ | Modifying program status word system mask, access key, and address space code system with overlap enabled - has register device coupled to execution unit and to queue device for storing standardised program status word, which is program status word in subsystem | |
| 136 | JP 06125275 A | ☒ | Signal processing device with A=D converter for e.g. magnetic recording/reproducing device - has circuits for analog input, reference signal detection and thermometer signal generation | |
| 137 | EP 614550 B | ☒ | Self-programming microcontroller with stored instruction to command program - uses instruction to program the program memory and autoincrementing pointer and on-chip ROM used to store program | |
| 138 | EP 539827 A | ☒ | Dynamic instruction modifying controller for computer - includes execution device and memory having control program which communicates to execution unit via conductor | |
| 139 | EP 565712 B | ☒ | Network structure for parallel processing computer programs - uses large number of highly efficient virtual processors derived from large memory banks in the core of the network | |
| 140 | US 5202964 A | ☒ | Interface controller including messaging scanner accessing state action table - has peripheral unit state changes detected in scanning mode to access state action table for assembling program addresses and microcodes | |
| 141 | EP 525666 A | ☒ | Information-processing microcomputer with branch target instruction buffer - transfers selected branch target instruction immediately to execution unit without waste of bus cycle during fetch | |
| 142 | EP 507066 A | ☒ | Ownership interlock for caches in data processing systems - prevents any processor ownership change to occur for cache data unit until all outstanding stores have been made | |
| 143 | US 5142630 A | ☒ | Instruction precontrol system for data processing unit - calculates branch destination address based on address mode bit in operand before executing instruction with changes address mode and branching | |
| 144 | EP 497485 A | ☒ | Data processing system with two operand instruction implementation - does not write result produced by operation to memory if destination value is unchanged | |

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| 145 | US 5113514 A | ☒ | Multiple-level multiprocessor cache memory organisation method - defining status of each cache with tag bit and updating tag bits with instruction execution | |
| 146 | EP 453268 A | ☒ | Microprocessor for inserting bus cycle to output internal information - has bus controller coupled to other processors to enable insertion of bus cycle in accordance with bus cycle request signal | |
| 147 | EP 450462 A | ☒ | Method for updating stored program information in ROM - using normal mode to down load information from ROM and changing to programming mode reprogramming memory | |
| 148 | EP 445479 A | ☒ | Peripheral sub-system for bulk memory - uses automatic peripheral controller to off load central processor in handling multiple bulk storage devices | |
| 149 | US 5226130 A | ☒ | Branch prediction cache with maintained consistency - organises store into instruction stream detection resulting in invalidation of corresponding cache entry data and main memory access | |
| 150 | EP 431326 A | ☒ | Inter-processor for MP computer system - generates interrupt request if zero is not detected on all low data being written to memory | |
| 151 | EP 419174 A | ☒ | Improved data processor with microprogram control - includes microinstruction execution unit which operates its pipeline process and resumes operation by using corrected parameters | |
| 152 | EP 408431 A | ☒ | Storage and restoration of modifiable programme executed by processor - uses read only memory to store executable code for program units and reprogrammable memory to store program modifications | |
| 153 | EP 401763 A | ☒ | Control timing signal generator - for mobile telephone performed by both absolute and relative time, and suitable for equipment control requiring numerous timing signals | |
| 154 | DE 4012347 A | ☒ | VCR remote controller memory addressing appts. - modifies RAM data by storing group initial addresses to form executable instructions | |
| 155 | EP 388526 A | ☒ | Programmable channel error inspection method and appts. - with means to time recovery of inspected errors is used for testing data processing system | |
| 156 | EP 380858 A | ☒ | Error handling method for pipelined computer system - distinguishes between errors that prevent instructions completing and those that do affect instructions | |
| 157 | EP 365188 A | ☒ | Programmable computer executing contiguous instructions in sequence - reduces delays in response to branch instructions using separate updated condition codes determined from previous instructions | |
| 158 | EP 363567 A | ☒ | Computer system with interrupt controlled clock speed - has machine language program which changes speed of oscillator clock when interrupt is generated | |
| 159 | US 4914584 A | ☒ | Intermediate code memory for buffering code segments - is located between main memory and processor to prefetch code and supply in-line instruction stream to processor | |
| 160 | EP 359233 A | ☒ | Computer system and method for changing operation speed of system bus - generates frequency change instruction in response to execution of program, and has sytem bus operation clock with variable frequency | |
| 161 | EP 327195 A | ☒ | Application program processor simulating data processor - reduces number of translated instructions needed to simulate flow of control of instructions | |
| 162 | EP 319132 A | ☒ | Data processing system for handling interrupts - allows interrupts to be handed while providing concurrent execution of instructions | |
| 163 | EP 315275 A | ☒ | Flexible ASIC microcomputer - has random access memory user defined dedicated functions and programmable read only memory | |
| 164 | AU 8818790 A | ☒ | Measurement of instruction execution for computer program - has selected instruction replaced with measurement instruction with indication of selected execution then restores and executes original | |

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| 165 | EP 297895 A | ☒ | Main memory updating in multiprocessor system - provides read, mask, add, quad word, interlocked instruction to synchronise loading or augmenting of data elements in main memory | |
| 166 | EP 297890 A | ☒ | Data processor fault condition response system - generates boolean valve indicating operation validity for storage at predetermined register position to initiate fault condition signal | |
| 167 | EP 275170 A | ☒ | Instruction decoder for variable byte processor - enables processing of different operands stored at different addresses by repeating operation, addresses being specified sequentially | |
| 168 | EP 270125 A | ☒ | High speed pipeline control system for calculator - divides instruction into several states and processes it so respective stages are operated in parallel to each other | |
| 169 | EP 265148 A | ☒ | Operating microprocessor controlled device e.g. bar code reader - by directly manipulating memory locations in microprocessor hardware by scanning bar code tags selected from menu | |
| 170 | EP 255186 A | ☒ | Parallel processing system for functional languages - has processors executing side effecting instructions modifying memory contents and functional instructions for locations in main memory | |
| 171 | EP 239081 A | ☒ | Pipelined data processor for parallel processing - has pair of instruction registers storing two instructions to be executed | |
| 172 | EP 230038 A | ☒ | Data processor address generation system - has correction number generator to modify contents of register in instruction execution unit according to instruction code address field | |
| 173 | EP 228242 A | ☒ | Non-intrusive microprocessor performance monitoring system - measures time spent at various parts of address space, in code execution and data accessing without altering real-time functions | |
| 174 | US 4675810 A | ☒ | Digital data processing system with organised memory system - uses object-based addressing having operand data identified by names accessed by name tables | |
| 175 | EP 207666 A | ☒ | Moving string of bytes instruction in reduced instruction set computer - using compiler to generate optimised sequences instead of hardware to perform operations and pre-compute operands | |
| 176 | EP 189202 A | ☒ | Microprogram control system - restores original micro instruction and assigned address by combining modified micro instructions and assigned addresses | |
| 177 | DE 3585517 G | ☒ | Microprocessor with variable memory capacity - uses bus changeover circuit which allows control of effective bit-width of data bus | |
| 178 | EP 170284 A | ☒ | Microcomputer processing data stored in different register banks - executes single instruction using logic gates and selector circuits to effect data transfers among banks | |
| 179 | SU 1174930 A | ☒ | Diagnostic and control unit - has control switches taken across address register to memory at inputs of logic conditions switch and comparator | |
| 180 | WO 8503150 A | ☒ | Data processing system with memory hierarchy - has ROM for storing program to be executed, changeable memory for storing instructions to change program, and RAM for revised program | |
| 181 | US 4494188 A | ☒ | Multiprocessor system operating method - dividing system into concurrently executable units and checking whether ready state process is present for each unit | |
| 182 | RD 249043 A | ☒ | Execute instruction to no-operation changing using linkage editor - having evaluated address constant added to execute instruction when NOP is required | |
| 183 | DE 3415209 A | ☒ | Data processor software security - address portion of instruction is modified when fetched from memory and restored before execution | |
| 184 | US 4434464 A | ☒ | Memory protection system for data processing system - effects alteration of protection information without intervention of control program when erroneous access is accepted | |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 185 | EP 97234 A | ☒ | Computer restarting system following normal or abnormal termination - maintains completion and operational states respectively of two structures w.r.t. subset of resource managers | |
| 186 | DE 32026 11 A | ☒ | Computer processor simulation system - uses replacement of major part of processors control logic by variable memory controlled via programmable register to deliver control signal | |
| 187 | EP 66376 A | ☒ | Data processing system with instruction buffer - pre-transfers instructions from main storage to buffer which is invalidated only when changed content is executed as instruction | |
| 188 | EP 59018 A | ☒ | Multi-programmed data processing system with dynamic task assignment - requiring no centralised interrogation of all data processing devices | |
| 189 | US 42875 61 A | ☒ | Address formulation interlock mechanism for processing system - uses two register identifying fields each having pre-decoded instruction entered into instruction queue | |
| 190 | US 41842 01 A | ☒ | Integrating processor preventing data dissemination - executes instructions from internal memory which cannot be accessed by input-output processor | |
| 191 | DE 28170 73 A | ☒ | Address processing for stored microinstructions of data processor - using address field modifier enabling prepared, direct and mixed linking modes | |
| 192 | US 40952 78 A | ☒ | Instruction altering system for program control system - has multiplexer switched by coincidence output of comparator circuit | |
| 193 | US 39407 45 A | ☒ | Computer with multiple hardware circuits - for processing at different priorities switched by priority change microinstruction | |
| 194 | FR 22608 29 A | ☒ | Data processing method - has microprogrammes transferring and correcting memories and registers | |
| 195 | US 38919 72 A | ☐ | Synchronous sequential controller for logic outputs - has medium scale integrated ccts. and logic gates connected together | |

| | L # | Hits | Search Text | DBs |
|---|---|---|---|---|
| 1 | L2 | 3542 | ((chang$3 alter$3 modif$6 overwrit$3) near10 (instruction code)).ab,ti. | USPAT; US-PGPUB |
| 2 | L4 | 14410 | (chang$3 alter$3 modif$6 overwrit$3) near10 ((instruction code) near20 (memory cache location address)) | USPAT; US-PGPUB |
| 3 | L6 | 2604 | execut$3 near30 4 | USPAT; US-PGPUB |
| 4 | L8 | 522 | (chang$3 alter$3 modif$6 overwrit$3) near10 ((instruction code) near20 (memory cache location address)) near30 execut$3 | EPO; JPO; DERWENT; IBM_TDB |
| 5 | L9 | 22638 | ((chang$3 alter$3 modif$6 overwrit$3) near10 (instruction code)).ab,ti. | EPO; JPO; DERWENT; IBM_TDB |
| 6 | L10 | 458 | 8 and 9 | EPO; JPO; DERWENT; IBM_TDB |
| 7 | L11 | 5 | 8 and patch$3 | EPO; JPO; DERWENT; IBM_TDB |
| 8 | L12 | 2657 | (chang$3 alter$3 modif$6 overwrit$3) near10 ((microinstruction microcode instruction code) near20 (memory cache location address)) near30 execut$3 | USPAT; US-PGPUB |
| 9 | L13 | 3 | 2 and 12 not 7 | USPAT; US-PGPUB |
| 10 | L15 | 423 | (chang$3 alter$3 modif$6 overwrit$3) near10 ((microinstruction microcode instruction code) near10 (memory cache location address)) near10 execut$3 | EPO; JPO; DERWENT; IBM_TDB |
| 11 | L16 | 195 | (chang$3 alter$3 modif$6 overwrit$3) near10 ((microinstruction microcode instruction code) near10 (memory cache location address)) near10 execut$3 | EPO; DERWENT; IBM_TDB |
| 12 | L7 | 385 | 2 and 6 | USPAT; US-PGPUB |
| 13 | L17 | 187 | 7 and @pd<19991006 | USPAT; US-PGPUB |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 1 | US 20040 01568 0 A1 | ☐ | Data processor for modifying and executing operation of instruction code | 712/226 |
| 2 | US 20030 17731 5 A1 | ☒ | Prefetch with intent to store mechanism | 711/137 |
| 3 | US 20030 16366 7 A1 | ☒ | Vector processing system | 712/7 |
| 4 | US 20030 15446 5 A1 | ☒ | Method and system for verifying modules destined for generating circuits | 717/137 |
| 5 | US 20030 13584 8 A1 | ☒ | Use of multiple procedure entry and/or exit points to improve instruction scheduling | 717/158 |
| 6 | US 20030 12641 4 A1 | ☒ | Processing partial register writes in an out-of order processor | 712/225 |
| 7 | US 20030 12088 0 A1 | ☒ | System having read-modify-write unit | 711/155 |
| 8 | US 20020 13870 2 A1 | ☒ | Using non-executable memory as executable memory | 711/154 |
| 9 | US 20020 08335 5 A1 | ☒ | Method and apparatus for dynamic power control of a low power processor | 713/322 |
| 10 | US 20010 04491 3 A1 | ☒ | Multiprocessor application interface requiring no ultilization of a multiprocessor operating system | 714/33 |
| 11 | US 66810 58 B1 | ☒ | Method and apparatus for estimating feature values in a region of a sequence of images | 382/294 |
| 12 | US 66683 15 B1 | ☒ | Methods and apparatus for exchanging the contents of registers | 712/219 |
| 13 | US 66657 08 B1 | ☒ | Coarse grained determination of data dependence between parallel executed jobs in an information processing system | 709/215 |
| 14 | US 66403 15 B1 | ☒ | Method and apparatus for enhancing instruction level parallelism | 714/17 |
| 15 | US 65500 00 B1 | ☒ | Processor to execute in parallel plurality of instructions using plurality of functional units, and instruction allocation controller | 712/215 |
| 16 | US 65428 91 B1 | ☒ | Safe strength reduction for Java synchronized procedures | 707/8 |
| 17 | US 65395 00 B1 | ☒ | System and method for tracing | 714/45 |
| 18 | US 65229 58 B1 | ☒ | Logic method and apparatus for textually displaying an original flight plan and a modified flight plan simultaneously | 701/3 |
| 19 | US 65197 07 B2 | ☒ | Method and apparatus for dynamic power control of a low power processor | 713/322 |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 20 | US 6425086 B1 | ☒ | Method and apparatus for dynamic power control of a low power processor | 713/322 |
| 21 | US 6345351 B1 | ☒ | Maintenance of speculative state of parallel executed jobs in an information processing system | 711/203 |
| 22 | US 6332206 B1 | ☒ | High-speed error correcting apparatus with efficient data transfer | 714/755 |
| 23 | US 6330657 B1 | ☒ | Pairing of micro instructions in the instruction queue | 712/23 |
| 24 | US 6308322 B1 | ☒ | Method and apparatus for reduction of indirect branch instruction overhead through use of target address hints | 717/145 |
| 25 | US 6286132 B1 | ☒ | Debugging support apparatus, a parallel execution information generation device, a computer-readable recording medium storing a debugging support program, and a computer-readable recording medium storing a parallel execution information generation program | 717/125 |
| 26 | US 6269440 B1 | ☒ | Accelerating vector processing using plural sequencers to process multiple loop iterations simultaneously | 712/241 |
| 27 | US 6249793 B1 | ☒ | Mostly concurrent compaction in a garbage collection system | 707/206 |
| 28 | US 6223335 B1 | ☒ | Platform independent double compare and swap operation | 717/100 |
| 29 | US 6178492 B1 | ☒ | Data processor capable of executing two instructions having operand interference at high speed in parallel | 712/23 |
| 30 | US 6112289 A | ☒ | Data processor | 712/23 |
| 31 | US 6009265 A | ☒ | Program product for optimizing parallel processing of database queries | 707/3 |
| 32 | US 6006316 A | ☒ | Performing SIMD shift and arithmetic operation in non-SIMD architecture by operation on packed data of sub-operands and carry over-correction | 712/22 |
| 33 | US 5974538 A | ☒ | Method and apparatus for annotating operands in a computer system with source instruction identifiers | 712/218 |
| 34 | US 5974240 A | ☒ | Method and system for buffering condition code data in a data processing system having out-of-order and speculative instruction execution | 712/218 |
| 35 | US 5940516 A | ☒ | Data security method and system | 713/159 |
| 36 | US 5937199 A | ☒ | User programmable interrupt mask with timeout for enhanced resource locking efficiency | 710/262 |
| 37 | US 5933497 A | ☒ | Apparatus and method for controlling access to software | 705/59 |
| 38 | US 5930807 A | ☒ | Apparatus and method for fast filtering read and write barrier operations in garbage collection system | 707/206 |
| 39 | US 5875342 A | ☒ | User programmable interrupt mask with timeout | 710/260 |
| 40 | US 5875337 A | ☒ | Modifier for a program executing parallel processes that reduces wait time for access to a shared resource | 717/151 |
| 41 | US 5850543 A | ☒ | Microprocessor with speculative instruction pipelining storing a speculative register value within branch target buffer for use in speculatively executing instructions after a return | 712/238 |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 42 | US 5832272 A | ☒ | Apparatus and method for parallel computation | 717/149 |
| 43 | US 5822608 A | ☒ | Associative parallel processing system | 712/20 |
| 44 | US 5815723 A | ☒ | Picket autonomy on a SIMD machine | 712/20 |
| 45 | US 5815421 A | ☒ | Method for transposing a two-dimensional array | 708/520 |
| 46 | US 5809292 A | ☒ | Floating point for simid array machine | 712/222 |
| 47 | US 5802338 A | ☒ | Method of self-parallelizing and self-parallelizing multiprocessor using the method | 712/217 |
| 48 | US 5757432 A | ☒ | Manipulating video and audio signals using a processor which supports SIMD instructions | 348/384.1 |
| 49 | US 5713012 A | ☒ | Microprocessor | 712/233 |
| 50 | US 5691724 A | ☒ | Police traffic radar using FFT processing to find fastest target | 342/104 |
| 51 | US 5659794 A | ☒ | System architecture for improved network input/output processing | 710/1 |
| 52 | US 5652852 A | ☒ | Processor for discriminating between compressed and non-compressed program code, with prefetching, decoding and execution of compressed code in parallel with the decoding, with modified target branch addresses accommodated at run time | 712/208 |
| 53 | US 5634047 A | ☒ | Method for executing branch instructions by processing loop end conditions in a second processor | 712/241 |
| 54 | US 5628024 A | ☒ | Computer architecture capable of concurrent issuance and execution of general purpose multiple instructions | 712/23 |
| 55 | US 5570093 A | ☒ | Police traffic radar using absolute signal strength information to improve target signal processing accuracy | 342/104 |
| 56 | US 5565871 A | ☒ | Police traffic radar for allowing manual rejection of incorrect patrol speed display | 342/176 |
| 57 | US 5563603 A | ☒ | Police traffic radar using digital data transfer between antenna and counting unit | 342/115 |
| 58 | US 5528245 A | ☒ | Police traffic radar using double balanced mixer for even order harmonic suppression | 342/104 |
| 59 | US 5525996 A | ☒ | Police traffic radar for calculating and simultaneously displaying fastest target speed | 342/104 |
| 60 | US 5515535 A | ☒ | System and method for parallel variable optimization | 717/149 |
| 61 | US 5511207 A | ☒ | Program control circuit determining the designated number of times a sequence of instructions is repetitively executed to prevent further execution of a jump instruction | 712/241 |
| 62 | US 5504843 A | ☒ | Apparatus and method for processing a stream of image data in a printing system | 358/1.16 |
| 63 | US 5440703 A | ☒ | System and method for saving state information in a multi-execution unit processor when interruptable instructions are identified | 712/228 |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 1 | US 20030 16367 9 A1 | ☐ | Method and apparatus for loop buffering digital signal processing instructions | 712/241 |
| 2 | US 20030 13134 2 A1 | ☐ | Debugger with activity alert | 717/125 |
| 3 | US 65981 55 B1 | ☐ | Method and apparatus for loop buffering digital signal processing instructions | 712/241 |
| 4 | US 60063 16 A | ☐ | Performing SIMD shift and arithmetic operation in non-SIMD architecture by operation on packed data of sub-operands and carry over-correction | 712/22 |
| 5 | US 58549 35 A | ☐ | Program transformation system for microcomputer and microcomputer employing transformed program | 717/159 |
| 6 | US 58128 13 A | ☐ | Apparatus and method for of register changes during execution of a micro instruction tracking sequence | 712/218 |
| 7 | US 57685 74 A | ☐ | Microprocessor using an instruction field to expand the condition flags and a computer system employing the microprocessor | 712/226 |
| 8 | US 57519 85 A | ☐ | Processor structure and method for tracking instruction status to maintain precise state | 712/218 |
| 9 | US 54817 05 A | ☐ | Method for executing a program with branch-to modifying instructions | 717/136 |
| 10 | US 54737 43 A | ☐ | Character generator with selectable conversion | 345/471 |
| 11 | US 54210 06 A | ☐ | Method and apparatus for assessing integrity of computer system software | 714/36 |
| 12 | US 49721 31 A | ☐ | Method of an apparatus for controlling velocity of industrial robot | 318/568 .1 |
| 13 | US 49185 93 A | ☐ | Relational database system | 707/200 |
| 14 | US 41842 00 A | ☐ | Integrating I/O element | 713/200 |
| 15 | US 35933 13 A | ☐ | CALCULATOR APPARATUS | 708/440 |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 64 | US 5416913 A | ☒ | Method and apparatus for dependency checking in a multi-pipelined microprocessor | 712/216 |
| 65 | US 5347639 A | ☒ | Self-parallelizing computer system and method | 712/203 |
| 66 | US 5151991 A | ☒ | Parallelization compile method and system | 717/150 |
| 67 | US 5088034 A | ☒ | Compiling method for determining programs to be executed parallelly by respective processors in a parallel computer which transfer data with a data identifier to other processors | 717/160 |
| 68 | US 5056004 A | ☒ | Program control system which simultaneously executes a program to be repeated and decrements repetition numbers | 712/241 |
| 69 | US 4843540 A | ☒ | Parallel processing method | 712/11 |
| 70 | US 4829422 A | ☒ | Control of multiple processors executing in parallel regions | 718/106 |
| 71 | US 4825360 A | ☒ | System and method for parallel processing with mostly functional languages | 718/106 |
| 72 | US 4498136 A | ☒ | Interrupt processor | 710/262 |
| 73 | US 4486830 A | ☐ | Programmable control apparatus and method | 700/17 |
| 74 | US 4412303 A | ☒ | Array processor architecture | 712/16 |
| 75 | US 4365292 A | ☒ | Array processor architecture connection network | 712/14 |
| 76 | US 4344134 A | ☒ | Partitionable parallel processor | 712/16 |
| 77 | US 4176395 A | ☐ | Interactive irrigation control system | 700/284 |
| 78 | US 3704453 A | ☒ | CATENATED FILES | 710/21 |

| | Document ID | U | Title | Current OR |
|---|---|---|---|---|
| 1 | US 20030028757 A1 | ☐ | Concurrent modification and execution of instructions | 712/226 |
| 2 | US 6651163 B1 | ☒ | Exception handling with reduced overhead in a multithreaded multiprocessing system | 712/244 |
| 3 | US 6574725 B1 | ☒ | Method and mechanism for speculatively executing threads of instructions | 712/31 |
| 4 | US 6202199 B1 | ☒ | System and method for remotely analyzing the execution of computer programs | 717/125 |
| 5 | US 6052528 A | ☒ | Process for managing the multiple inheritance of persistent and shared objects | 717/116 |
| 6 | US 5999734 A | ☒ | Compiler-oriented apparatus for parallel compilation, simulation and execution of computer programs and hardware models | 717/149 |
| 7 | US 5694604 A | ☒ | Preemptive multithreading computer system with clock activated interrupt | 718/107 |
| 8 | US 5675776 A | ☒ | Data processor using FIFO memories for routing operations to parallel operational units | 712/220 |
| 9 | US 5414822 A | ☒ | Method and apparatus for branch prediction using branch prediction table with improved branch prediction effectiveness | 712/240 |
| 10 | US 5333188 A | ☒ | Effective address pre-calculation type pipelined microprocessor | 711/214 |
| 11 | US 4561052 A | ☒ | Instruction prefetch system | 712/207 |
| 12 | US 4109311 A | ☒ | Instruction execution modification mechanism for time slice controlled data processors | 712/226 |
| 13 | US 4084235 A | ☒ | Emulation apparatus | 703/26 |
| 14 | US 3593313 A | ☒ | CALCULATOR APPARATUS | 708/440 |